Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA) – France
Institut de recherche sur leslois fondamentales de l'Univers

DESIGN OF A MONOLITHIC SILICON PIXEL DETECTOR WITH ADAPTIVE RATE FOR PARTICLE PHYSICS

In current and future high-energy physics experiments, the use of multi-channel submicron integrated circuits has become a standard for both vertexing and tracking systems. In particular, "Monolithic Active Pixel Sensor" (MAPS) technology, where pixel sizes can be as small as 10 x 10 μm^2. This high granularity allows reaching record spatial resolutions with minimal dead areas, and the development of MAPS technology opened the road to high radiation tolerance with limited power consumption. However, modern silicon pixel detectors operate in a high occupancy environment requiring a fast readout (up to 40 Mframes/s), thus they pay the price of a huge quantity of data to be handled. This large amount of data is acceptable where a maximum spatial resolution is required, but can be prohibitive when this is not necessary, or when space and consumption constraints put limits on the number of fast downstream links. Therefore, each experiment or application require to redefine the combination of the pixel size and the architecture of the detector's readout electronics, to meet the occupancy rate requirements of each physics environment in terms of detector's readout capabilities.

A major innovation in the design of silicon sensors for particle physics relies on the decoupling of the pixel matrix from the chip periphery which houses the readout and defines the actual data rate. Our team has been working on MAPS detectors for high energy particle physics experiments since 2003 and is now devoting a relevant part of its R&D on the development of a generic data compression readout circuit to adapt the sensor performance to the typical high occupancy environment of the High-Luminosity LHC. Within this thesis work, the candidate is expected to develop two complementary approaches aiming at reducing the final data rate sent out by the readout circuitry of the sensor: 1. Grouping pixels or cluster of pixels within the so-called "virtual pixels"; 2. Implement an adaptive "on-chip" architecture based on neural networks. While this exploratory study aims at providing a technological solution which enhances the generality and energy efficiency of the readout implementation, a specific application case will be considered as a benchmark. This case is the Upstream Tracker detector of the LHCb experiment a CERN, which is going to be upgraded in the coming years to cope with the challenging conditions of the High Luminosity LHC.

Based on the ongoing design of MAPS, developed in collaboration with CERN and CNRS, the candidate will first focus on the development of a compression algorithm which will be iteratively validated in simulations. Then, the chosen algorithm will undergo the phase of the HDL implementation into the electronics simulation to assess its actual performances, particularly in terms of computing and power cost. Finally, the "circuit signoff" phase will consist in developing an actual micro-electronics design in VLSI, leading to the production of chip vehicles which will be extensively tested in lab and in beam.

The proposed thesis is fully funded for a duration of 3 years and will be performed within the PHENICS Doctoral School of the Paris Saclay University.

The applicants should send a CV and a motivation letter to the contacts below not later than May 31st 2024.

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